of FIG. 10.

FIGs. 15A to 15E are cross-sectional views of a manufacturing method of a thin film transistor array panel according to the third embodiment of the present invention.

FIG. 16A shows cross-sectional and plane views of a gate pad in a thin film transistor array panel for a liquid crystal display according to a fourth embodiment of the present invention.

FIG. 16B shows cross-sectional and plane views of a data pad in a thin film transistor array panel for a liquid crystal display according to the fourth embodiment of the present invention.

FIGs. 17A to 17D are cross-sectional views of a manufacturing method of a thin film transistor array panel according to the fourth embodiment of the present invention.

FIG. 18 is a layout view of a thin film transistor array panel for a liquid crystal display according to a fifth embodiment of the present invention.

FIG. 19 is a cross-sectional view taken along line XIX-XIX' of FIG. 18.

FIG. 20 is a layout view of a thin film transistor array panel for a liquid crystal display according to a sixth embodiment of the present invention.

FIG. 21 is a cross-sectional view taken along line XXI-XXI' of FIG. 20.

FIG. 22 is a layout view of a thin film transistor array panel for a liquid crystal display according to a seventh embodiment of the present invention.

FIG. 23 is a cross-sectional view taken along line XXIII-XXIII' of FIG. 22.

FIGs. 24A to 24B are cross-sectional views of a manufacturing method